UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,354	12/08/2003	Kuang-Feng Sung	10465-US-PA	1353

31561 7590 01/10/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
WELLS, KENNETH B

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,354	SUNG, KUANG-FENG	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The disclosure is objected to because of the following informalities: the specification is replete with grammatical errors too numerous to mention specifically (e.g., in paragraph 0005, the first sentence and the last line thereof). All such errors should be corrected in response to this office action.

Appropriate correction is required.

2. Claims 1-8 are objected to because of the following informalities: in claim 1, it appears that "decayed" should actually be --delayed--(note also that this problem occurs throughout the specification). On line 3 of claim 1, "a main output stage" should be changed to --the main output stage-- for purposes of proper antecedent basis. On line 6 of claim 5, "the switches" lacks antecedent basis. In claims 7 and 8, line 2 of each, "is" should be changed to --are--. Appropriate correction is required.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the

> invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Okamoto et al.

As to claim 1, note Fig. 7, where the recited "main output stage" reads on circuit 2 (the "main current" is the current through either inverter I1 or inverter I2); the recited "monitoring stage" reads on the series-connected FETs N2 and N3 (the recited "delayed push/pull signals" read on the pull-up/down currents output provided by FETs N2 and N3, respectively); and the recited "assistant output stage" reads on inverter I5 (its output push-pull currents are provided to the node between inverters I2 and I3).

As to claim 2, the output from inverter I5 to the main output stage 2 is a "feedback" current in the same manner that applicant's assistant current is a feedback current, i.e., in both Okamoto et al's Fig. 7 and instant Figs. 2 and 3, the assistant current is generated in response to an output from the main output stage and is provided to an output node of the main output stage.

As to claim 3, the current through inverter I1 is interpreted as the "main current" (it begins to flow prior to

the flow of current through inverter I5 due to the delay function of FETs N2, N3 and also the internal delay of inverter I1).

Alternatively regarding claim 3, and also regarding claim 4, note that the "main current" flowing through the inverter I1 or I2 in Fig. 7 of Okamoto et al is constantly flowing (the push/pull currents through these inverters are constantly going on and off due to the on/off of their CMOS transistors). Thus, the "main current" (through either the pull-up or pull-down FETs within inverters I1 and I2) is constantly turning on and then turning off during operation of the Fig. 7 circuit in Okamoto et al. Because of this, the "assistant current" output from inverter I5 will be both on and off after the main current within circuit 2 is flowing.

4. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Hidaka et al.

As to claims 1 and 2, note Fig. 3, where the recited "main output stage" reads on the push-pull pair of FETs 1a and 2a; the recited "monitoring stage" reads on the combination of delay 12b and gates 13b, 14b; and the recited "assistant output stage" reads on the push-pull pair of FETs 1b, 2b.

As to claims 3 and 4, note the above discussion of the main and assistant currents which are constantly turning on and then turning off during operation of the Fig. 3 circuit in Hidaka et al. Because of this, the "assistant current" output by FETs 1b and 2b will be both on and off after the "main current" output by FETs 1a and 2a.

As to claims 5 and 6, note Fig. 80A of Hidaka et al, where the detecting of first and second inputs occurs due to the action of differential amplifier 490; the push and pull currents are through FETs 492 and 494, respectively; the feedback of the push-pull currents (claim 6) is from the common drains of FETs 492,494 to the non-inverting input of amplifier 490. The "main current" is merely intended use in the preamble of claim 5 and cannot be relied upon to define over Hidaka et al.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka et al.

The "main current" of claims 7 and 8 can be interpreted as any current in an overall larger integrated circuit that the Fig. 80A output circuit is used in (because no relationship has been defined between the push-pull currents and the main current). It would have been obvious to one of ordinary skill in the art that such an output circuit is for use in such an IC within, for example, a computer system (the motivation is to obtain the benefits of the Fig. 80A circuit taught by Hidaka et al). Because the other (i.e., "main") currents of a computer system would be constantly turning on/off before and after the currents through FETs 492 and 494 when this circuit is used in an overall larger integrated circuit, claims 7 and 8 do not define patentable subject matter under 35 USC 103.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner

can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

January 5, 2005